What is Claimed Is:

1. An encoding system comprising:

means for Manchester encoding a data value to produce a coded data value;

means for producing a first invalid Manchester encoded sequence as a start of frame signal; and

means for producing a transmission packet including the start of frame code followed by the coded data value.

2. The encoding system according to claim 1 wherein the start of frame signal is a sequence of "110110".

3. The encoding system according to claim 1 further comprising:

means for producing a second invalid Manchester encoded sequence as an end of frame code; and

means for including the end of frame code in the transmission packet after the coded data value.

4. The encoding system according to claim 3 wherein the end of frame signal is a sequence of "001000".

5. The encoding system according to claim 1 wherein the end of frame signal includes a valid Manchester code.

6. The encoding system according to claim 1 wherein the start of frame signal includes a valid Manchester code.

7. An encoding system comprising:

means for Manchester encoding a data value to produce a coded data value;

means for producing a first invalid Manchester encoded sequence as a start of frame code;

means for producing a second valid Manchester encoded sequence as an end of frame code; and

means for producing a transmission packet including the start of frame code followed by the coded data value followed by the end of frame code.

8. The encoding system according to claim 7 wherein the end of frame code is a sequence of "001000".

9. The encoding system according to claim 7 wherein the start of frame code is a sequence of "110110".

10. A decoding system comprising:

receiving means for receiving a first Manchester encoded signal including a first start of frame code followed by first coded data values, the first start of frame code is a valid Manchester code; and

means for detecting the first start of frame code to determine a beginning of the first coded data values in the first Manchester encoded signal.

11. The decoding system according to claim 10 wherein the first start of frame code is a sequence of "110110".

12. The decoding system according to claim 10 wherein the Manchester encoded signal includes a first end of frame code following the first

coded data values, the first end of frame code is a valid Manchester code, and the decoding system further comprising means for detecting the first end of frame code to determine an end of the first coded data values in the first Manchester encoded signal.

13. The decoding system according to claim 12 wherein the first end of frame code is a sequence of "001000".

14. The decoding system according to claim 12 wherein the receiving means includes means for receiving a second Manchester encoded signal including a second start of frame code followed by second coded data values, the second start of frame code is a valid Manchester code and the decoding system further comprises means for determining that the first Manchester encoded data is invalid if the second start of frame code is received before the first end of frame code.

15. An integrator comprising:

receiving means for receiving a first signal including a first data value and a second data value different from the first data value;

counter means for increasing a count value when the first signal includes the first data value and decreasing the count value when the first signal includes the second data value;

data means for producing a third data value when the count value is equal to or greater than a first threshold value and a fourth data value when the count value is equal to or less than a second threshold value; and

signal generating means for producing a second signal including the third data value and the fourth data value.

16. The integrator according to claim 15 further comprising a low pass filter comprising the counter means, the data means, and the signal generating means.

17. The integrator according to claim 15 wherein the counter means includes means for preventing the count value from exceeding a maximum value which is greater than or equal to the first threshold value.

18. The integrator according to claim 15 wherein the counter means includes means for preventing the count value from exceeding a minimum value which is less than or equal to the second threshold value.

19. A discriminator comprising:

receiving means for receiving a first signal including a first data value and a second data value different from the first data value;

counter means for increasing a count value when the first signal includes the first data value and resetting the count value to a predetermined value when the first signal includes the second data value; and

clock synchronization means for producing a clock synchronization signal when the count value is equal to or greater than a first threshold value.

20. The discriminator according to claim 17 further comprising data means for producing a third data value when the count value is equal to or greater than the first threshold value and a fourth data value when the count value is reset.

21. The integrator according to claim 19 wherein the counter means includes means for preventing the count value from exceeding a maximum value which is greater than or equal to the first threshold value.

22. A decoder comprising:

an integrator including:

(a) receiving means for receiving a first signal including a first data value and a second data value different from the first data value,

(b) first counter means for increasing a first count value when the first signal includes the first data value and decreasing the first count value when the first signal includes the second data value,

(c) data means for producing a third data value when the first count value is equal to or greater than a first threshold value and a fourth data value when the first count value is equal to or less than a second threshold value, and

(d) signal generating means for producing a second signal including the third data value and the fourth data value; and

a discriminator including:

(a) second counter means for increasing a second count value when the second signal includes the third data value and resetting the second count value to a predetermined value when the second signal includes the fourth data value, and

(b) clock synchronization means for producing a clock synchronization signal when the second count value is equal to or greater than a third threshold value.

23. The decoder according to claim 22 further comprising data means for producing third signal including a fifth data value when the count value is equal to or greater than the first threshold value and a sixth data value when the count value is reset.

24. The decoder according to claim 23 further comprising decoding means for decoding the first signal in response to the third signal and the clock synchronization means.